Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Claims 1-25. (Cancelled)

Claim 26. (New) A power supply for providing power from a battery having a positive terminal and negative terminal to a load having a first terminal and a second terminal, wherein the second terminal of the load is coupled to the negative terminal of the battery, the power supply comprising:

an inductor, wherein a first terminal of the inductor is coupled to the positive terminal of the battery;

a first transistor, wherein a gate of the first transistor is coupled to a first pulse generator, a drain of the first transistor is coupled to a second terminal of the inductor, and a source of the first transistor is coupled to the negative terminal of the battery;

a second transistor, wherein a drain of the second transistor is coupled to the second terminal of the inductor and a gate of the second transistor is coupled to a source of the second transistor, and the source of the second transistor is coupled to the first terminal of the load; and

a third transistor, wherein a gate of the third transistor is coupled to a second pulse generator, a drain of the third transistor is coupled to the source of the second transistor, and a source of the third transistor is coupled to the negative terminal of the battery.

Claim 27. (New) The power supply of claim 26, wherein the first and third transistors are NMOS transistors and the second transistor is a PMOS transistor.

Claim 28. (New) The power supply of claim 26, further comprising a fourth transistor, wherein a drain of the fourth transistor is coupled to the source of the second transistor, a gate of the fourth transistor is coupled to the second pulse generator, and a source of the fourth transistor is coupled to the gate of the second transistor and to the drain of the third transistor.

Claim 29. (New) The power supply of claim 28, wherein the fourth transistor is a PMOS transistor.

Claim 30. (New) The power supply of claim 26, further comprising:

a capacitor, wherein a first terminal of the capacitor is coupled to the positive terminal of the battery and a second terminal of the capacitor is coupled to the negative terminal of the battery.

Claim 31. (New) The power supply of claim 26, further comprising:

a capacitor, wherein a first terminal of the capacitor is coupled to the source of the second transistor and a second terminal of the capacitor is coupled to the negative terminal of the battery.

Claim 32. (New) The power supply of claim 26, wherein the first pulse generator is adapted to generate a plurality of pulses, wherein each of the plurality of pulses is used to store charge in the inductor.

Claim 33. (New) The power supply of claim 26, wherein the second pulse generator is adapted to generate a plurality of pulses, wherein each of the plurality of pulses is used to release charge stored in the inductor into the load.

Claim 34. (New) The power supply of claim 26, wherein the first pulse generator and the second pulse generator are controlled by a power controller.

Claim 35. (New) The power supply of claim 26, wherein the battery is a battery cell.

Claim 36. (New) A power supply for providing power from first and second batteries, each having a positive terminal and negative terminal, to a load having a first terminal and a second terminal, wherein the second terminal of the load is coupled to the negative terminals of the first and second batteries, the power supply comprising:

a first inductor, wherein a first terminal of the first inductor is coupled to the positive terminal of the first battery;

a second inductor, wherein a first terminal of the second inductor is coupled to the positive terminal of the second battery; and

first and second controlled power switches, the first controlled power switch coupled to a second terminal of the first inductor and the positive and negative terminals of the first battery and the second controlled power switch coupled to a second terminal of the second inductor and the positive and negative terminals of the second battery, the first controlled power switches comprising

a first transistor, wherein a gate of the first transistor is coupled to a first pulse generator, a drain of the first transistor is coupled to the second terminal of the first inductor, and a source of the first transistor is coupled to the negative terminal of the first battery,

a second transistor, wherein a drain of the second transistor is coupled to the second terminal of the first inductor, a gate of the second transistor is coupled to a source of the second transistor, and the source of the second transistor is coupled to the first terminal of the load, and

a third transistor, wherein a gate of the third transistor is coupled to a second pulse generator, a drain of the third transistor is coupled to the source of the second transistor, and a source of the third transistor is coupled to the negative terminal of the first battery.

Claim 37. (New) The power supply of claim 36, wherein the first and third transistors are NMOS transistors and the second transistor is a PMOS transistor.

Claim 38. (New) The power supply of claim 36, wherein the first controlled power switch further comprises a fourth transistor, wherein a drain of the fourth

transistor is coupled to the source of the second transistor, a gate of the fourth transistor is coupled to the second pulse generator, and a source of the fourth transistor is coupled to the gate of the second transistor and to the drain of the third transistor.

Claim 39. (New) The power supply of claim 38, wherein the fourth transistor is a PMOS transistor.

Claim 40. (New) The power supply of claim 36, further comprising:

a first capacitor, wherein a first terminal of the first capacitor is coupled to the positive terminal of the first battery and a second terminal of the first capacitor is coupled to the negative terminal of the first battery; and

a second capacitor, wherein a first terminal of the second capacitor is coupled to the positive terminal of the second battery and a second terminal of the second capacitor is coupled to the negative terminal of the second battery.

Claim 41. (New) The power supply of claim 36, further comprising:

a first capacitor, wherein a first terminal of the first capacitor is coupled to the first controlled power switch and a second terminal of the first capacitor is coupled to the negative terminal of the first battery; and

a second capacitor, wherein a first terminal of the second capacitor is coupled to the second controlled power switch and a second terminal of the second capacitor is coupled to the negative terminal of the second battery.

Claim 42. (New) The power supply of claim 36, wherein the first pulse generator is adapted to generate a plurality of pulses, wherein each of the plurality of pulses is used to store charge in the first inductor.

Claim 43. (New) The power supply of claim 36, wherein the second pulse generator is adapted to generate a plurality of pulses, wherein each of the plurality of pulses is used to release charge stored in the first inductor into the load.

Claim 44. (New) The power supply of claim 36, wherein the first pulse generator and the second pulse generator are controlled by a power controller.

Claim 45. (New) The power supply of claim 36, wherein each of the first and second batteries is a battery cell.

Claim 46. (New) The power supply of claim 36, wherein the second controlled power switches comprises:

a fourth transistor, wherein a gate of the fourth transistor is coupled to a third pulse generator, a drain of the fourth transistor is coupled to the second terminal of the second inductor, and a source of the fourth transistor is coupled to the negative terminal of the second battery,

a fifth transistor, wherein a drain of the fifth transistor is coupled to the second terminal of the second inductor, a gate of the fifth transistor is coupled to a source of the

fifth transistor, and the source of the fifth transistor is coupled to the first terminal of the load, and

a sixth transistor, wherein a gate of the sixth transistor is coupled to a second pulse generator, a drain of the sixth transistor is coupled to the source of the fifth transistor, and a source of the sixth transistor is coupled to the negative terminal of the second battery.